REMARKS

This application contains claims 1-9, 11-19 and newly added claim 21. Claims 10 and 20 have been cancelled. Claims 1, 7, 11 and 17 have been amended herein.

Claims 1-20 were rejected under 35 U.S.C. 101. Claims 1 and 11 have been amended herein to be directed to the execution of a computer program. Claim 1 now recites: a method for executing a computer program. Claim 11 is now directed to a computing system that executes a computer program. After examining the tag associated with a given instruction, and if such associated tag has been set, branching to the translated version of the given instruction, for further execution of the program occurs.

The Examiner's reliance on the Guidelines is simply wrong. It is pointed out to the Examiner that MPEP § 2106 states:

> **These Guidelines do not constitute substantive rulemaking and hence do not have the force and effect of law. These Guidelines have been designed to assist *>USPTO< personnel in analyzing claimed subject matter for compliance with substantive law.**

The execution of a computer program, and the specific manner in which it is done, is exactly the type of "useful, concrete and tangible result" contemplated by the United States Court of Appeals for the Federal Circuit in State Street Bank & Trust C. v. Signature Financial Group, Inc., 47 U.S.P.Q.2d 1596. Although the Guidelines are not

controlling law, even the Guidelines state, with respect to the case cited above:

> The claimed invention as a whole must >be useful and< accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." *State Street*, 149 F.3d at *>1373-74<, 47 USPQ2d at 1601-02. ***The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research*** (*Brenner v. Manson*, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96 **> (1966); *In re Fisher*, 421 F.3d 1365, 76 USPQ2d 1225 (Fed. Cir. 2005); *In re Ziegler*, 992 F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)) (emphasis added).

It is submitted that claim 1 produces such a "real world" practical result; that is the execution of a computer program. To hold that claim 1 is not directed to patentable subject matter would be in effect to hold that no method for the operation of a programmed digital computer would ever be patentable, a result clearly at odds with the issuance of many patents covering new, useful and not obvious ways in which a computer may execute a program. It is submitted that claim 11 is also clearly directed to patentable subject matter.

Claim 1 recites a computing system that executes a computer program. Claim 1 also recites various means, which refer to both hardware and software embodiments, as disclosed in the specification. If the Examiner's rejection of claim 1 is taken to its logical conclusion, then no claim directed to

a computer system could ever be patentable; a result not supported in law or fact.

It is thus submitted that claims 1-20 are directed to patentable subject matter, under 35 U.S.C. 101.

Claims 1-20 were rejected under 35 U.S.C. 103(a) as being obvious over Bala in view of Fu et al. In view of the amendments made herein, and the remarks below, these rejections are respectfully traversed.

Applicants' invention, as set forth in claim 1, as amended herein, is directed to in a computing system that executes a computer program, including dynamic compilation capability, a method for controlling the execution of an instruction of the computer program. The method comprises the steps of translating an instruction from a first representation to a translated representation, and setting a tag associated with the instruction in the first representation; and prior to execution of a given instruction in the first representation, examining the tag associated with the given instruction, and if such associated tag has been set, branching to the translated version of the given instruction, for further execution of the program, and if the tag has not been set, interpreting and compiling the given instruction from the first representation, for further execution of the program. Significantly, the examining of the tag is effected without performing a cache fetch.

Support for the current amendment, discussed below, may be found, throughout the specification, and in particular in Fig. 1 (see for example, branching to 100), and the description in the specification at paragraphs [0028] to [0033] of applicant's published application.

In Applicant's prior paper, specific reference was made to paragraph [0061] of applicant's published application (approximately page 15 as filed), wherein it is noted that applicants' invention is an improvement over prior art systems because:

"prior art switching suffers either excessive memory consumption requirements if a switch monitor as described in May, op. cit., is used wherein a switch entry is associated with each instruction address, or from massive hardware requirements if all known entries are to be stored in a CAM memory structure, or from slow performance if all migrant instruction addresses must be read from cache/memory. The present invention improves on these prior techniques because the determination of whether a translation exists can be effected by the relatively fast technique of examining a field within the code tag associated with an instruction, rather than perform a cache fetch for possible translated versions in each case. Therefore, the current invention improves switch detection and translation without unduly degrading performance or posing massive hardware requirements."

It was noted in Applicant's prior paper that this is in sharp contrast to Bala, wherein the tag "hits" are the

presence of translated code in a cache (see Bala, column 1, lines 43-48 and column 3, lines 22-30).

It is noted that the Examiner has now attempted to combine the teachings of Bala with Fu et al. However, it is submitted that this is an improper combination of references. First, Fu et al. simply deal with processing ordered data requests to a memory, and has nothing whatsoever to do with dynamic compiling or translating code from a first representation to a second representation. Second, Fu et al. deals with prefetches and the case when there is a miss in memory, and not with the examining of the tag being effected without performing a cache fetch. In other words, in Fu et al., when it is known that there will be a miss, then a prefetch is needed to find data. In Applicant's invention, if a tag is not set, it indicates that there is no translation of the code, and a prefetch is simply irrelevant and unnecessary, and time can be saved by not even attempting a fetch. The Examiner's reasoning simply does not address these reasons for why it is not obvious to combine Bala and Fu et al.

For this reason alone, it is submitted that claim 1 is directed to patentable subject matter. However, claim 1 has also been amended, as noted above, to recite: if the tag has not been set, interpreting and compiling the given instruction from the first representation, for further execution of the program. Neither Bala nor Fu et al., whether taken alone or in combination, teach or suggest, based on the status of the tag, returning to the first representation, and interpreting and executing it. This

provides the advantage of a fast and efficient way to continue executing the program, without undue burden in terms of additional operations and computational overhead, which could be required if additional translation were attempted. Thus, this is a second reason for why claim 1 is patentable over the combination of Bala and Fu et al.

In view of the above, it is respectfully submitted that claim 1 is directed to patentable subject matter.

Apparatus claim 11 has been amended in a manner analogous to method claim 1. For the reasons set forth with respect to claim 1, it is respectfully submitted that claim 11 is also directed to patentable subject matter.

Newly added claim 21, which depends from claim 11, notes that the system further comprising an exception handler for execution of the program when an exception in the translated representation occurs. This enables the system to deal with certain difficulties, which may occur in the system environment. Support for this claim may be found in, among other places, Fig. 1 (item 114), and paragraph [0034] of Applicant's published specification. Neither Bala nor Fu et al. teach or suggest an exception handler. It is thus submitted that claim 21 is directed to patentable subject matter.

The remaining claims depend from one of the independent claims discussed above. These claims have further recitations, which in combination with those of the

claim from which they depend, are not taught or suggested by the art of record.

It is respectfully submitted that the Examiner is simply wrong with respect to claims 7 and 17, which have been amended to recite that the tag is a single bit. Reference is made to Bala, column 3, and throughout. The undersigned could find no teaching or suggestion that the tag is a single bit. In fact the teachings of column 3 of Bala suggest that cache hit or miss signals would have more than a single bit. The Examiner admits as much in the rejection of claims 8 and 18. There is a patentable distinction between the hit signal, and the tag, as Bela clearly teaches that the tags comprise multiple bits. It is a major advantage, in terms of efficiency of storage for the tag to be a single bit, as in claims 7 and 17. Thus, it is submitted that the rejection of claims 7 and 17 is simply wrong, as it is not supported in fact or law.

A check in the amount of $1,020 is enclosed for a three-month extension of time required for the filing of this paper and the associated RCE.

Respectfully submitted,

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